

ROUTING ALGORITHMS IN NETWORKS-ON-CHIP

David Brindle

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Cluster Based Hierarchical Routing Algorithm for Network on Chip

This work is devoted to the study of communication subsystem of networks-on-chip (NoCs) development with an emphasis on their topologies.

USB2 - Router design for 3D network-on-chip - Google Patents

This book provides a single-source reference to routing algorithms for Networks-on-Chip (NoCs), as well as in-depth discussions of advanced solutions applied.

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Network on a chip - Wikipedia

Every system has its own requirements for the routing algorithm. This report looks through the basics of networking

on Network on Chip systems and presents.

Cluster Based Hierarchical Routing Algorithm for Network on Chip

and compared. Keywords—Network on Chip, Router, XY routing algorithm, interconnections and mostly shared busses are used for onchip communication.

ABSTRACT. This paper introduces a new, practical routing algorithm, Maze- routing, to tolerate faults in network-on-chips. The algorithm is the first to provide all.

Routing Algorithms in Network on Chip" submitted by "Jayant Kumar Singh" algorithms are compared i.e. one deterministic routing (XY routing algorithm).

ERA: An Efficient Routing Algorithm for Power, . Throughput and Latency in Network-on-Chips. Varsha Sharma, Rekha Agarwal. Manoj S Gaur, Vijay Laxmi, and.

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Techniques for optimizing design of a hard intellectual property block for data transmission. It seems that you're in Germany. Unlike tri-gate or multiplexer based crossbar arrays conventionally used in a NOC router, the present embodiment, Routing Algorithms in Networks-on-Chip transmission gates or pass transistors, is designed to be fast, compact low area and consume less power than a conventional router. Retrieved Notes Electr. The latched address bits are then compared with the coordinate of the local router and appropriate output ports are selected adaptively.

EPA2en.Developmentofauniversaladaptivefastalgorithmforthesynthesis Routing design specific global on chip wires for system-on-chip SOCs can be costly and inefficient.